

Abstract of the Disclosure

A semiconductor apparatus is composed of a signal providing circuit and a data analyzer. The signal providing circuit provides an input signal set including at least one input signal. The data analyzer outputs a digital result signal in synchronization with a clock signal. The data analyzer inverts the digital result signal at a timing indicated by the clock signal while the input signal set is in a predetermined state, and does not invert the digital result signal while the input signal set is not in the predetermined state.

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